FIG.1

FIG.2A

HIGHER
LAYERS
AND
APPLICATIONS
207

HOST
205

HOST I/O
AND
LINK
MANAGER
209

LINK
CONTROLLER
211

RADIO
213

BLUETOOTH DEVICE
203

215

FIG.2B

HIGHER
LAYERS
AND
APPLICATIONS
227

L2CAP
LAYER
229

HCI
LAYER
231

HOST
225

PHYSICAL INTERFACE
233

HOST
CONTROLLER
237

LINK
MANAGER
239

LINK
CONTROLLER
241

RADIO
243

BLUETOOTH DEVICE
235

223

FIG.2C

FIG.3

```
                              301
                        M  303
                       /│\
                      / │ \
                     /  │  \
          305       /   │   \        309
           S       S  • • • •  S
                  307
```

FIG.4

```
          403
           M₁               401
           │
           M  405            407
          /│\               /\
         / │ \             /  \
   409  /  │  \           /    \  415
    S   S   \         M      S
        411  \       / \
              S ──── S   
             413
```

FIG.5

FIG.6

601

TIME · · ·

| T | R | T | R | T | R | · · · |

603 605 607 609

HV1 PACKETS

611

TIME · · ·

| T | R | T | R | T | R |

613 615 617 619

HV2 PACKETS

621

TIME · · ·

| T | R | T | R |

623 625 627 629

NO FEC

HV3 PACKETS

FIG.7

713 — CODE C

703 — L2CAP
701

702 — HCl

HOST

SCO PATH

709 — HCl

LINK MANAGER — 705

715

707

PHYSICAL

FIG.8

801

803 — L2CAP

805 — HCl

807 — USB

809 — USB

811 — HCl

FIRMWARE

813 — PHYSICAL

FIG.9

```
                                                            ┌─ 901
┌──────────────────────────────────────────────────────────┐
│                                                            │
│      ┌─ 903                      ┌─ 905                     │
│   ┌────────────────┐          ┌────────────────┐           │
│   │     L2CAP      │          │     L2CAP      │           │
│   │    TRANSMIT    │          │    RECEIVE     │           │
│   └────────────────┘          └────────────────┘           │
│      ┌─ 907                      ┌─ 909                     │
│   ┌────────────────┐          ┌────────────────┐           │
│   │      SCO       │          │      SCO       │           │
│   │    TRANSMIT    │          │    RECEIVE     │           │
│   └────────────────┘          └────────────────┘           │
│      ┌─ 911                      ┌─ 913                     │
│   ┌────────────────┐          ┌────────────────┐           │
│   │      LMP       │          │      LMP       │           │
│   │    TRANSMIT    │          │    RECEIVE     │           │
│   └────────────────┘          └────────────────┘           │
│                                                            │
└──────────────────────────────────────────────────────────┘
```

09/788061.021601

FIG.10

PROTECT BIT ARRAY

1011 1001 1003

0	FRAGMENT 127 (EMPTY)	
	⋮	
1	FRAGMENT 7 (IN USE)	
0	FRAGMENT 6 (EMPTY)	
0	FRAGMENT 5 (EMPTY)	
1	FRAGMENT 4 (IN USE)	
1	FRAGMENT 3 (IN USE)	
1	FRAGMENT 2 (IN USE)	
1	FRAGMENT 1 (IN USE)	
1	FRAGMENT 0 (IN USE)	

1015

1013

7 BITS	127
⋮	
7	4
	3
4	2
	1
2	0

1005 — BASE POINTER (X10)

1006 — FORWARD POINTER (X10)

READ POINTERS

1007 — WRITE POINTER (X10)

64 BYTES

1009

FIG.11

1103 1105 1107 1101

FF	LF	LENGTH	◄— BYTE 0
L_CH	FB		◄— BYTE 1
			◄— BYTE 63

1109 1111

FIG.12

FIG.13

FIG.14

1401

FIRMWARE-GENERATED HEADERS FOR PACKETS AND FRAGMENTS
Tx FIFO

1403 — HCI LAYER

1405

| FIRMWARE PACKET #1 | FIRMWARE PACKET #2 |
| 124 BYTES | 124 BYTES |

FIRMWARE PACKETS

1407 1409

| 61-BYTE PAYLOAD | 63-BYTE PAYLOAD | 61-BYTE PAYLOAD | 63-BYTE PAYLOAD | 61-BYTE PAYLOAD | 63-BYTE PAYLOAD |

FRAGMENTS

| BB PACKET PAYLOAD #1 DM3, 121 BYTES | BB PACKET PAYLOAD #2 DM3, 121 BYTES | BB PACKET PAYLOAD #3 DM3, 121 BYTES |

BB PACKETS FORMED BY SEGMENTER

1411

HARDWARE-GENERATED HEADERS

FF=1 LF=1 FRAGMENT LENGTH=63
L_CH=01
LENGTH =124
FF=0 LF=1 FRAGMENT LENGTH=63

FLW
TYPE
HEC(5:0)
AM_ADDR
ARQ SEQ
HEC(7:6)

⟶ t

| | TX | RX | TX | RX | TX | RX | TX | RX |
| | BB PACKET #1 DM3 | DM1 | SCO TX | SCO TX | BB PACKET #1 DM3 | DM1 | SCO TX | SCO TX |

1413

RX EVENT FOR DM1

FLW
TYPE
HEC(5:0)
AM_ADDR
ARQ SEQ
HEC(7:6)

ARQ=1

*RX EVENT FOR DM1
*TX CONFIRMATION EVENT FOR FIRMWARE PACKET #1

BEGINNING OF WRITE OPERATIONS

END OF WRITE OPERATIONS

FLW
TYPE
HEC(5:0)
AM_ADDR
ARQ SEQ
HEC(7:6)

ARQ=1

FIG.15

```
                              ╱│╲  ─── 1525                    ─── 1523
          ┌─────────────────────────────────────────────────┐
          │ BLUETOOTH RF                                      │
          │   ┌─────────────────────────────────────────┐    │
          │   │                RF/IF                     │    │
          │   └─────────────────────────────────────────┘    │
          └─────────────────────────────────────────────────┘
                              ⇕
          ┌─────────────────────────────────────────────────┐ ─── 1517
          │ BLUTOOTH BASEBAND                                │
          │   ┌─────────────────────────────────────────┐    │
          │   │         BASEBAND  CONTROLLER            │    │
1511 ───  │   └─────────────────────────────────────────┘    │ ─── 1515
          │   ┌──────────────────┐  ┌──────────────┐         │
          │   │                  │  │    LINK      │         │
          │   │                  │  │   MANAGE     │         │
          │   │  HCI HARDWARE    │  │  FIRMWARE    │         │
          │   │                  │  └──────────────┘         │ ─── 1513
          │   │                  │  ┌──────────────┐         │
          │   │                  │  │ HCI FIRMWARE │         │
          │   └──────────────────┘  └──────────────┘         │
          └─────────────────────────────────────────────────┘
1519 ───          ⇕          1521 ───        ⇕                 ─── 1509
          ┌─────────────────────────────────────────────────┐
          │          PHYSICAL BUS                            │
          │          HARDWARE                                │
          │   ┌─────────────────────────────────────────┐    │
          │   │   PHYSICAL BUS(USB PC CARD               │    │
          │   │      OTHER) FIRMWARE                     │    │
          │   └─────────────────────────────────────────┘    │
          └─────────────────────────────────────────────────┘
                              ⇕                               ─── 1501
          ┌─────────────────────────────────────────────────┐
          │ BLUTOOTH HOST                                    │
1507 ───  │   ┌─────────────────────────────────────────┐    │
          │   │   PHYSICAL BUS(USB PC CARD               │    │
          │   │      OTHER) DRIVER                       │    │
          │   └─────────────────────────────────────────┘    │
1505 ───  │   ┌─────────────────────────────────────────┐    │
          │   │           HCI DRIVER                     │    │
          │   └─────────────────────────────────────────┘    │
1503 ───  │   ┌─────────────────────────────────────────┐    │
          │   │   OTHER HIGHER LAYER DRIVER              │    │
          │   └─────────────────────────────────────────┘    │
          └─────────────────────────────────────────────────┘
```

09788061_021601

FIG.16

1601

BLUE RF INTERFACE — 1651 → RF

TRANSMIT DATA PATH — 1645 → TO RF

SEGMENTER/PACKET COMPOSER RETRANSMIT CONTROLLER FLUSHER — 1639

FREQUENCY HOPPER — 1653

TIMING CONTROL — 1655

POWER MANAGER — 1657

LINK CONTROL UNIT — 1647

RECEIVE DATA PATH — 1649 ← FROM RF

AUDIO PROCESSOR — 1641

FLOW CONTROL — 1649

LINK MANAGER — 1603

LMP TX FIFO — 1613, 1625

L2CAP TX FIFO — 1615, 1627

SCO TX FIFO — 1617, 1629

SCO CONTROLLER — 1607, 1633

SCO RX FIFO — 1631, 1635

L2CAP RX FIFO — 1619, 1621

LMP RX FIFO — 1623

UART/USB — 1605

PCM INTERFACE — 1607

UART/USB — 1605

LINK MANAGER — 1611

1637

FIG.17

FIG.18

FIG.19A

$$S_1(1) \rightarrow \quad 6 \quad 5 \quad 4 \quad 3 \quad 2 \quad 1 \quad 0 \quad n \quad n-1 \quad n-2 \quad n-3$$
$$S_2(1) \rightarrow \quad 6 \mid 5 \mid 4 \mid 3 \mid 2 \mid 1 \mid 0 \mid \boxed{n} \mid n-1 \mid n-2 \mid n-3 \mid$$

1951 1909 1903

$$S_1(2) \rightarrow \quad 8 \quad 7 \quad 6 \quad 5 \quad 4 \quad 3 \quad 2 \quad 1 \quad 0 \quad n \quad n-1$$
$$S_2(2) \rightarrow \quad 7 \mid 6 \mid 5 \mid 4 \mid 3 \mid 2 \mid 1 \mid 0 \mid -1 \mid \boxed{n-1} \mid n-2 \mid$$

1951 1911 1905

1947 1947 1907

$$S \quad \mid 6 \mid 5 \mid 4 \mid 3 \mid 2 \mid 1 \mid 0 \mid 0 \mid 0 \mid n-2 \mid n-3 \mid$$

$\phi = 312$

$S_{M,TX}$	5	4	3	2	1	0	0	0	0	n-3	n-4
$S_{M,RX}$	6	5	4	3	2	1	0	0	0	n-2	n-3
$S_{S,TX}$	6	5	4	3	2	1	0	2	1	n-2	n-3
$S_{S,RX}$	5	4	3	2	1	0	3	2	1	n-3	n-4

FIG.19B

1941
SLOT BOUNDARIES
1943
1945
BLUETOOTH CLOCK

625 usec

1947

FIG.20

TABLE 1. PACKET TYPE PRIORITY ⟶ 2001

RANGE LABEL	MIN BYTES IN BUFFER	MAX BYTES IN BUFFER	1ST. CHOICE	2ND. CHOICE	3RD. CHOICE	4TH. CHOICE	5TH. CHOICE	6TH. CHOICE
a	0	0	NULL	NULL	NULL	NULL	NULL	NULL
b	1	17	DM1	DH1	DM3	DH3	DM5	DH5
c	18	27	DH1	DM3	DH3	DM5	DH5	DM1
d	28	121	DM3	DH3	DM5	DH5	DH1	DM1
e	122	183	DH3	DM5	DH5	DM3	DH1	DM1
f	184	224	DM5	DH5	DH3	DM3	DH1	DM1
g	225	339	DH5	DM5	DH3	DM3	DH1	DM1
h	339		DH5	DM5	DH3	DM3	DH1	DM1

FIG.21

EXAMPLE OF A FRAGMENT CHOOSER FOR 16 FRAGMENTS, N=4
(FOR 127 FRAGMENTS N=7)
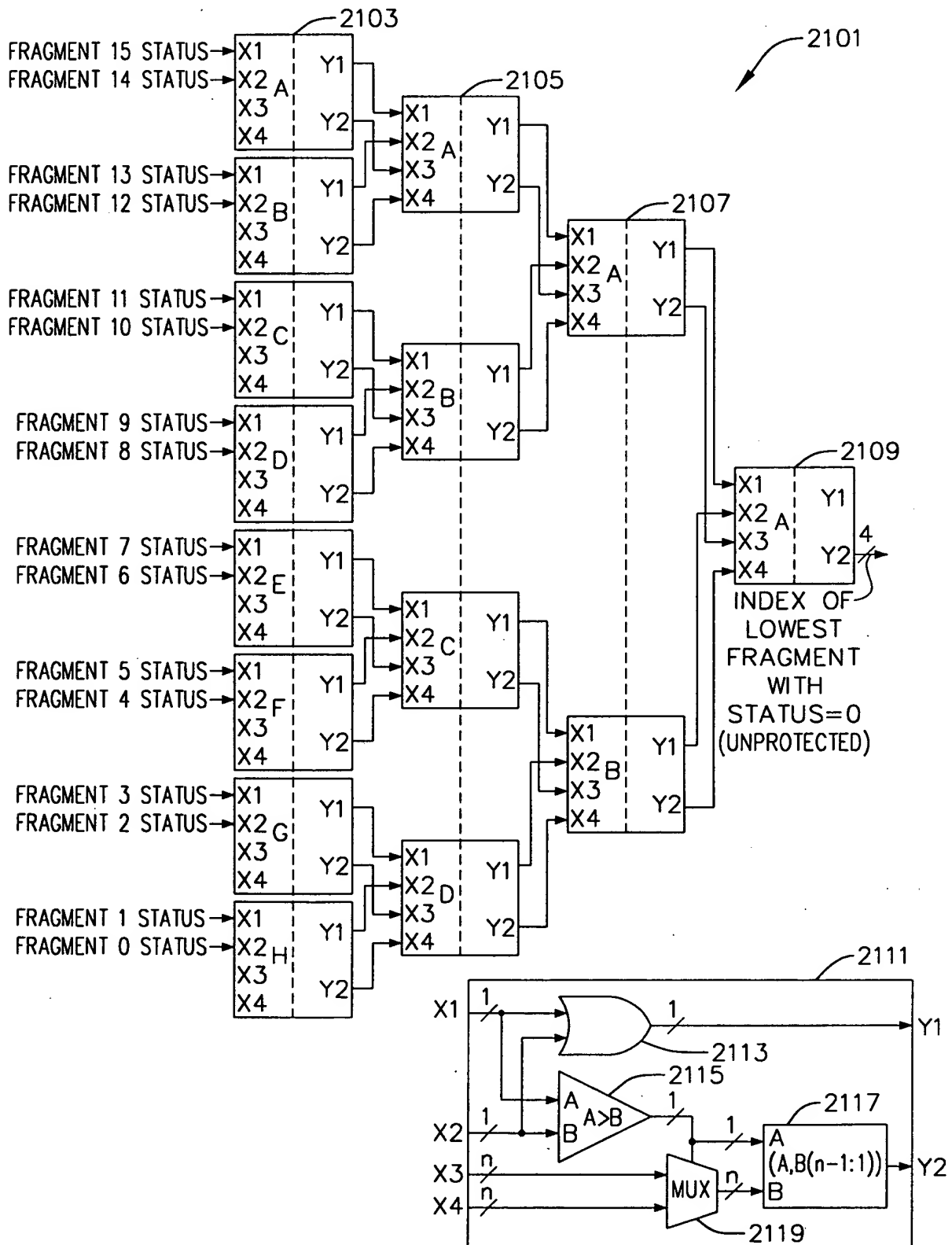
INDEX OF LOWEST FRAGMENT WITH STATUS=0 (UNPROTECTED)

FIG.22

CIRCUIT TO CALCULATE CLK MOD Y, WHERE CLK IS 27 BITS AND T IS 8 BITS

FIG.23

EXAMPLE CALCULATION: 115307261 MOD 135

```
2301

2305
   0 0 0 0 0 0 1 1 0 1 0 0 0 0 1 0 0 0 0 1 1 0 0 0 0 0        2307
1 0 0 0 0 1 1 1 | 1 1 0 1 1 0 1 1 1 1 1 0 1 1 1 0 0 1 0 1 1 1 1 1 1 0 1    2303
                  0 1 1 1 1 0 0 1
2309  t=9  ──►   0 1 0 1 0 1 0 0 1
                  1 0 1 1 1 1 0 0 1
      t=10 ──►   0 0 1 0 0 0 1 0 1
                   0 0 0 0 0 0 0 0
      t=11 ──►   0 1 0 0 0 1 0 1 1
                   1 0 1 1 1 1 0 0 1
      t=12 ──►   0 0 0 0 0 1 0 0 0
                   0 0 0 0 0 0 0 0
      t=13 ──►   0 0 0 0 1 0 0 0 1
                   0 0 0 0 0 0 0 0
      t=14 ──►   0 0 0 1 0 0 0 1 1
                   0 0 0 0 0 0 0 0
      t=15 ──►   0 0 1 0 0 0 1 1 1
                   0 0 0 0 0 0 0 0
      t=16 ──►   0 1 0 0 0 1 1 1 0
                   1 0 1 1 1 1 0 0 1
      t=17 ──►   0 0 0 0 0 1 1 1 0
                   0 0 0 0 0 0 0 0
      t=18 ──►   0 0 0 0 1 1 1 0 1
                   0 0 0 0 0 0 0 0
      t=19 ──►   0 0 0 1 1 1 0 1 0
                   0 0 0 0 0 0 0 0
      t=20 ──►   0 0 1 1 1 0 1 0 1
                   0 0 0 0 0 0 0 0
      t=21 ──►   0 1 1 1 0 1 0 1 1
                   1 0 1 1 1 1 0 0 1
      t=22 ──►   0 1 1 0 0 1 0 0 1
                   1 0 1 1 1 1 0 0 1
      t=23 ──►   0 1 0 0 0 0 1 0 1
                   0 0 0 0 0 0 0 0
      t=24 ──►   1 0 0 0 0 1 0 1 1
                   0 0 1 1 1 1 0 0 1
      t=25 ──►   1 0 0 0 0 1 0 0 1
                   0 1 0 1 1 1 0 0 1
      t=26 ──►   1 0 0 0 0 0 1 0 0
                   1 0 1 1 1 1 0 0 1
      t=27 ──►   0 1 1 1 1 1 0 1 1
                   1 0 1 1 1 1 0 0 1
                   0 0 1 1 1 0 1 0 0      2311
                       ANSWER
```

FIG.24

TX — 2403   RX — 2405   2401

ACK

2400

2417 (FRAGMENT N+5)

2429 WRITE PTR

2427 FORWARD PTR

READ DIRECTION

2415 (FRAGMENT N+4)

2413 (FRAGMENT N+3)

2419

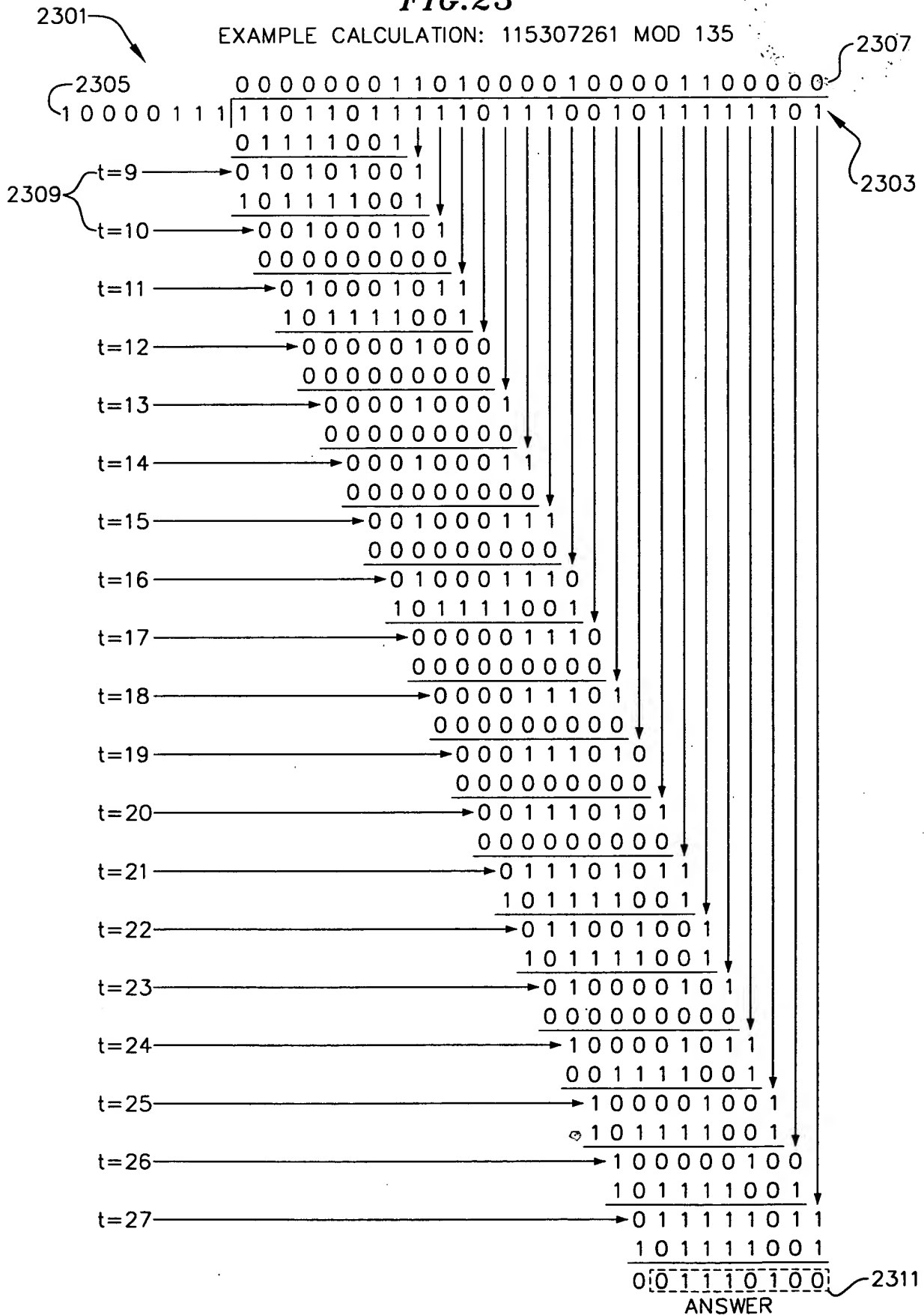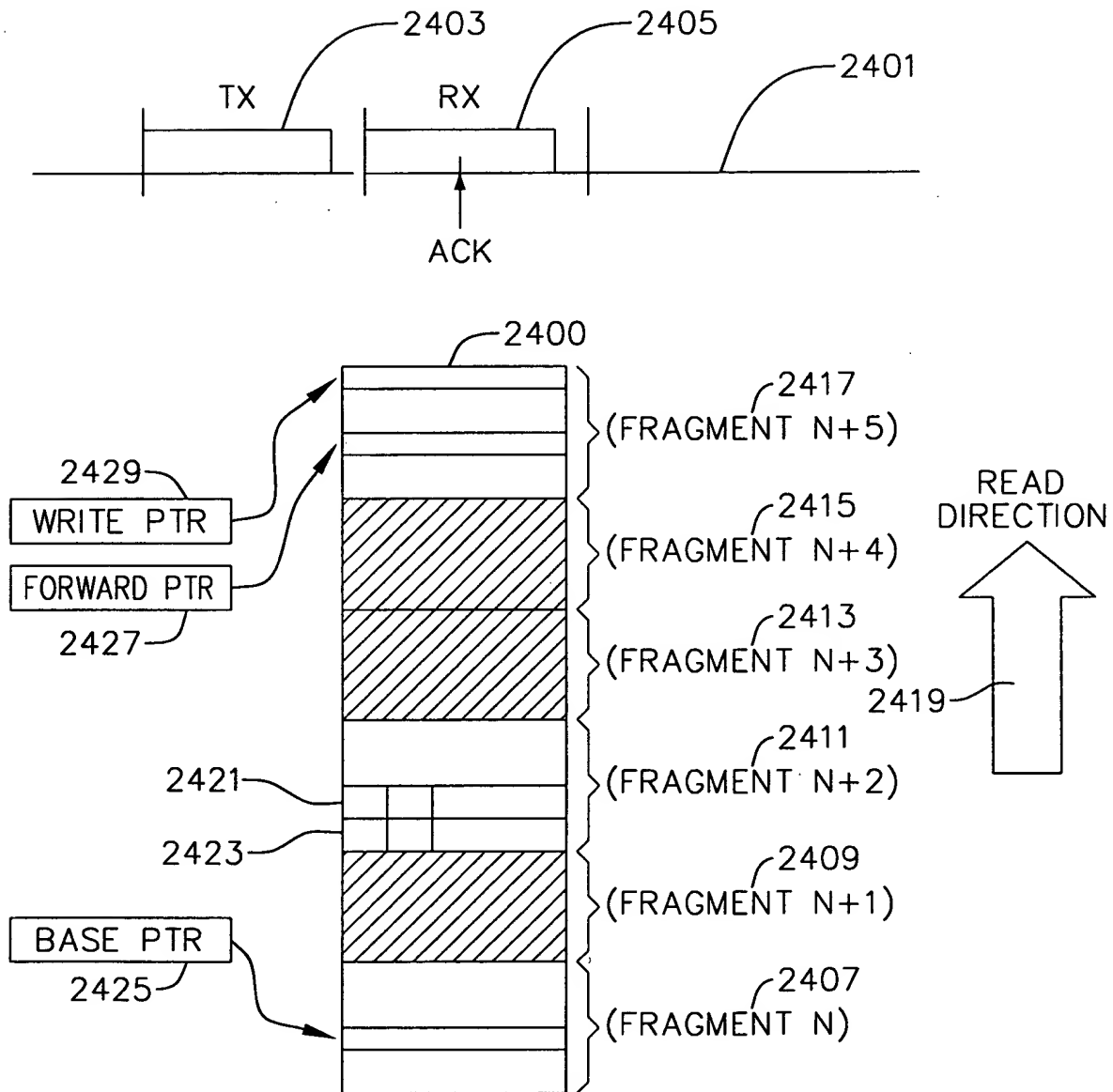2411 (FRAGMENT N+2)

2421
2423

2409 (FRAGMENT N+1)

BASE PTR
2425

2407 (FRAGMENT N)

FIG.25

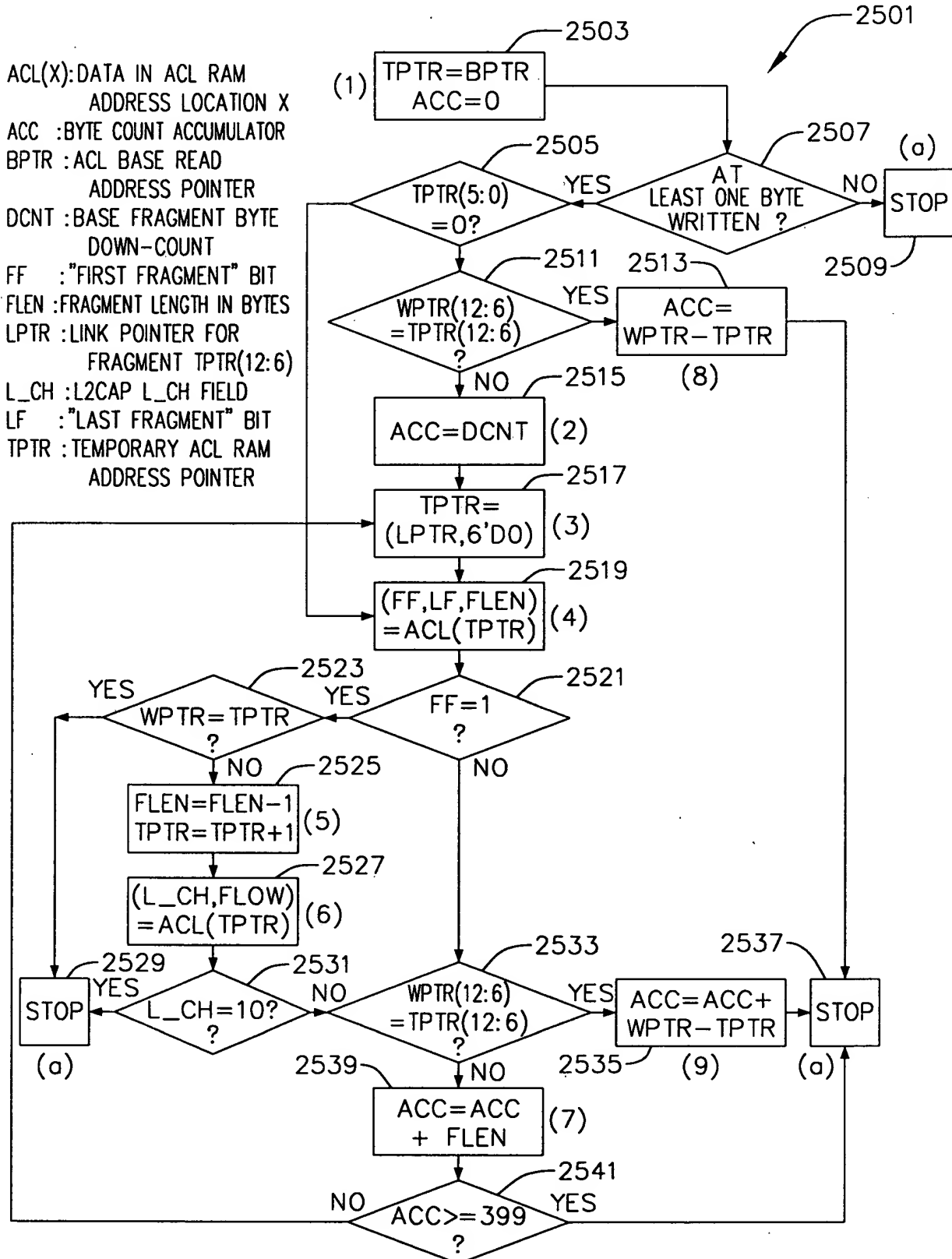THE FOLLOWING DIPICTS THE BYTE GAUGE STATE MACHINE IN FLOW DIAGRAM FORM. NUMBERS IN PARENTHESES INDICATE THE STATE.
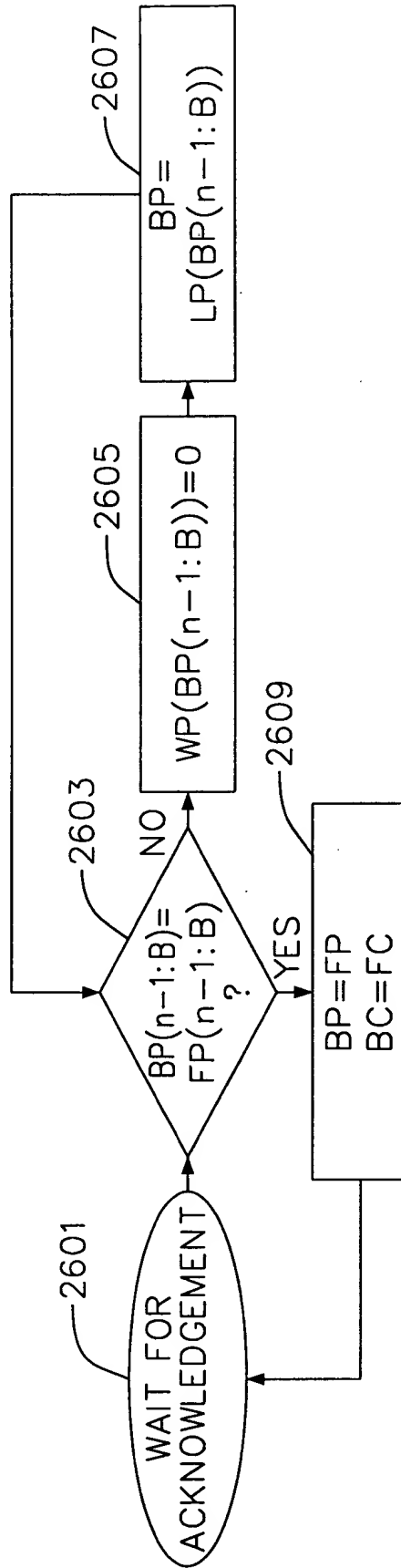
ACL(X): DATA IN ACL RAM
        ADDRESS LOCATION X
ACC : BYTE COUNT ACCUMULATOR
BPTR : ACL BASE READ
        ADDRESS POINTER
DCNT : BASE FRAGMENT BYTE
        DOWN-COUNT
FF   : "FIRST FRAGMENT" BIT
FLEN : FRAGMENT LENGTH IN BYTES
LPTR : LINK POINTER FOR
        FRAGMENT TPTR(12:6)
L_CH : L2CAP L_CH FIELD
LF   : "LAST FRAGMENT" BIT
TPTR : TEMPORARY ACL RAM
        ADDRESS POINTER

FIG.26

L2CAP PACKET FLUSH STATE MACHINE

2601 — WAIT FOR ACKNOWLEDGEMENT

2603 — $BP(n-1:B)=FP(n-1:B)$?

NO

2605 — $WP(BP(n-1:B))=0$

2607 — $BP=LP(BP(n-1:B))$

YES

2609 — $BP=FP$ $BC=FC$

FIG.27

L2CAP PACKET TRANSMIT STATE MACHINE

KEY:
BBH1: BASEBAND PACKET HEADER, 1ST. BYTE
BBH2: BASEBAND PACKET HEADER, 2ND. BYTE
BC : BASE DOWN-COUNT (COUNTS DOWN FROM FRAGMENT LENGTH)
BP : BASE POINTER
FC : FORWARD DOWN-COUNT (COUNTS DOWN FROM FRAGMENT LENGTH)
FP : FORWARD POINTER
LP : LINK POINTER ARRAY
MEM : L2CAP MEMORY ARRAY
N   : NUMBER OF BITS IN ADDRESS TO MEMORY ARRAY
PB : PAYLOAD BYTE DOWN-COUNT (COUNTS DOWN FROM PACKET LENGTH)
PLH1: PAYLOAD HEADER, 1ST. BYTE
PLH2: PAYLOAD HEADER, 2ND. BYTE
WP : WRITE PROTECTION ARRAY --ONE BIT PER FRAGMENT

NOTATION:
--   : DECREMENT BY ONE
++   : INCREMENT BY ONE
X(Y) : ELEMENT Y OF ARRAY X
A(B:C): BITS B THROUGH C OF N BIT BUS A
(D,E) : CONCATINATION OF D AND E
6'H   : 6-BIT HEX VALUE